A Low-Power Inverted Ladder D/A Converter

Yevgeny Perelman and Ran Ginosar

***Abstract*—Interpolating, dual resistor ladder digital-to-analog converters (DACs) typically use the fine, least significant bit (LSB) ladder floating upon the static most significant bit (MSB) ladder. The usage of the LSB ladder incurs a penalty in dynamic performance due to the added output resistance and switch matrix parasitic capacitance. Current biasing of the LSB ladder addresses this issue by employing active circuitry. We propose an inverted ladder DAC, where an MSB ladder slides upon two static LSB ladders. While using no active components this scheme achieves lower output resistance and parasitic capacitance for a given power budget. We present a 0.35-μm, 3.3-V implementation consuming 22-μA current with output resistance of 40 kΩ and effective parasitic capacitance of 650 fF.**

***Index Terms*—Digital-to-analog converter (DAC), low power, resistor ladder.**

I. Introduction

RESISTOR-STRING digital-to–analog converters (DACs) are the most basic of DAC families, typically suitable for midaccuracy applications (up to 10 bits). They are of special importance in processes with no high-quality capacitors available. Among their advantages are monotonicity, simple design and lack of active circuitry.

The drawback of a "straightforward" resistor ladder is the number of elements, resistors, and switches—2^N for N bits of accuracy. A large number of switches is particularly disturbing: apart of consuming area they load the ladder with parasitic capacitance and complicate the control logic.

The requirement for 2^N elements can be relaxed through interpolating the voltages of the coarse [most significant bit (MSB)] ladder by means of the second [fine, or least significant bit (LSB)] ladder [1]–[3]. If the coarse ladder provides N_c bits and the fine ladder – N_f bits, the overall complexity is reduced to $2^{N_c} + 2^{N_f}$.

Using a secondary ladder degrades the DAC differential nonlinearity (DNL), due to the finite ohmic load on the primary ladder. Static current flow through the secondary ladder causes a voltage drop on the interladder switches, increasing the DNL even further. The errors are introduced at the fine ladder end points.

Several techniques for isolating the fine ladder from the coarse ladder by means of active buffers are presented in [4]. The drawback of this approach is the requirement for two large common mode buffers, with offsets matched up to the required DAC accuracy over the whole output range. Bandwidth requirement on the buffers contributes to overall power consumption.

Manuscript received March 2, 2005; revised November 25, 2005. This paper was recommended by Associate Editor B. Zhao.

The authors are with the VLSI Systems Research Center, Department of Electrical Engineering, Technion–Israel Institute of Technology, Haifa 32000, Israel (e-mail: perelman@tx.technion.ac.il; ran@ee.technion.ac.il).

Digital Object Identifier 10.1109/TCSII.2006.875313

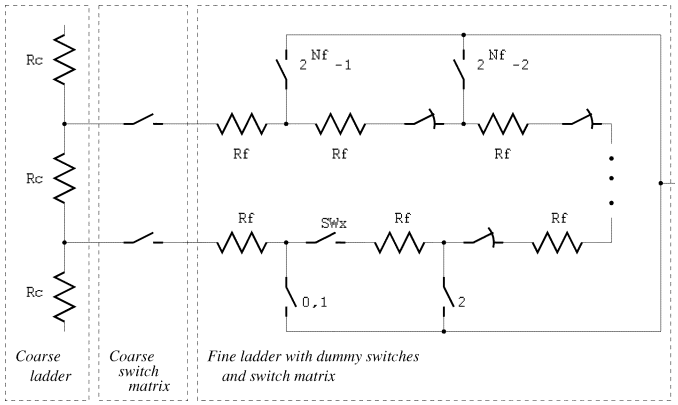


Fig. 1. Fine ladder compensation by dummy switches.

Compensating for the secondary ladder loading effects provides an alternative to isolation by active circuitry. While completely passive compensation is possible and will be reviewed below, it severely degrades the dynamic performance.

Pelgrom [2] suggested another passive compensation scheme which does not deteriorate the performance at the expense of a great increase in a switch matrix complexity, back to 2^N.

Maloberti *et al.* [3] proposed compensating the load by forcing a constant current through the fine ladder. Only dc active circuitry is involved, posing no bandwidth requirements; power penalty therefore is modest. The switch matrix complexity is maintained at $2^{N_c} + 2^{N_f}$.

This paper presents a novel resistor string DAC architecture with $2^{N_c} + 2^{N_f}$ switch complexity. The proposed architecture outperforms the existing circuits of the same complexity in terms of load driving ability and ladder parasitic capacitance under equal supply current.

The paper is organized as follows. Section II briefly reviews existing architectures of fine ladder compensation. Section III describes the proposed circuit. Simulation-based comparison between the mentioned architectures is presented in Section V. Silicon test of a prototype circuit incorporating the proposed DAC is described in Section VI. Finally, a brief summary concludes our discussion.

II. Existing Schemes for Fine Ladder Compensation

A. Passive Compensation

A possible solution to the aforementioned issues is shown in Fig. 1. Here the switch voltage drop is compensated by introducing dummy switches between the LSB ladder resistors. If dummy switches are identical to switches in the MSB switch matrix, every LSB ladder step includes an LSB resistor and a switch. LSB zero level is obtained at LSB tap number 1 when SWx switch is opened.

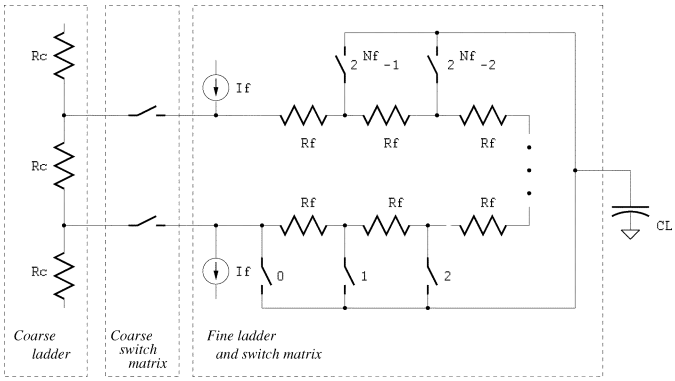


Fig. 2. Fine ladder current biasing compensation.

An ohmic load presented by the fine ladder to the coarse ladder is brought down to an acceptable level by choosing a sufficiently large fine ladder resistance. The condition to satisfy is keeping the coarse resistor voltage drop due to fine ladder loading below fraction α of an LSB

$$\frac{V_{\text{ref}}}{2^{N_c} \cdot R_c}(R_c - R_c \| (2^{N_f} R_f)) < \alpha \cdot \frac{V_{\text{ref}}}{2^N}$$

which can be further simplified to

$$R_f > \frac{R_c}{\alpha}. \tag{1}$$

This DAC will have maximal output resistance when both ladders are at the middle

$$r_o = \frac{R_c 2^{N_c}}{4} + \frac{R_f 2^{N_f}}{4}$$

if we substitute (1) and remember that the ladder current is

$$I = I_c = \frac{V_{\text{ref}}}{2^{N_c} R_c} \tag{2}$$

the output resistance becomes

$$r_o = \frac{V_{\text{ref}}}{4I}\left(1 + \frac{2^{N_f - N_c}}{\alpha}\right). \tag{3}$$

Equation (3) shows that a heavy penalty in dynamic performance is incurred when using the secondary ladder. As one will usually keep the DNL at least at half LSB (often at quarter LSB), and choose N_c approximately equal to N_f, r_o is increased by a factor of 2–5.

Further degradation of dynamic performance comes out of the dummy switches that contribute to capacitive loading on the fine ladder.

B. Compensation by Current Biasing

Fig. 2 shows a compensation scheme proposed in [3]. Ideally the current flowing through the fine ladder satisfies the condition

$$2^{N_f} \cdot R_f \cdot I_f = R_c \cdot I_c. \tag{4}$$

In that case, there is no current flow through MSB switches eliminating both the loading on the coarse ladder and the voltage drop on the MSB switch matrix.

The advantage of this scheme is that there is no need to satisfy (1). Instead, (4) has to be satisfied, which has a degree of freedom, I_c/I_f. Fine ladder resistance can be significantly decreased. Dummy switches are no longer needed, since there is no voltage drop on the MSB switch matrix to compensate for. The output resistance of this structure is

$$r_o = \frac{R_c 2^{N_c}}{4} + \frac{R_f 2^{N_f}}{4}.$$

Substituting (4) and (2)

$$r_o = \frac{V_{\text{ref}}}{4}\left(\frac{1}{2^{N_c} I_f} + \frac{1}{I_c}\right).$$

The current consumption is given by

$$I = I_c + I_f \cdot k.$$

Since I_f is generated by active circuitry there is more than a single branch carrying I_f, which is the reason for the presence of k. The circuit presented in [3] has $k = 3$.

Minimizing r_o under a given I leads to

$$r_o = \frac{V_{\text{ref}}}{4I} \cdot \left(1 + 2\sqrt{\frac{k}{2^{N_c}}}\right). \tag{5}$$

This is a dramatic improvement over (3): the increase in r_o due to the presence of fine ladder is much lower, 40%-60%.

The speed gain comes at the expense of added circuit complexity. Special circuitry is required for generating precise bias current to keep the ladders balanced. The currents at the top and the bottom of the ladder must be closely matched. Active generation of bias currents may pose some difficulty when the output voltage limits are close to supply rails. Bias generation circuitry will probably include additional elements requiring more current, not directly related to I_f (such as the OTA in [3]).

III. Proposed Novel Scheme

The proposed DAC architecture is shown in Fig. 3. For simplicity, we have shown a 10 bit DAC with $N_f = N_c = 5$. Unlike the existing schemes where the LSB ladder floats upon the coarse ladder, we suggest the exact opposite: a coarse ladder that slides upon *two LSB ladders*. Switches of the top and the bottom LSB ladders operate in parallel according to the lower five bits of the input word: for example, when these equal 11001, switch 25 is shortened in both the top and the bottom ladders. The MSB switches operate on the upper five bits of the input code, thus their numbers are shown in steps of 32. The total string resistance is therefore kept constant, independent of the LSB ladder position: an R_f resistance is added at the bottom and removed from the top at the same time. The current flow through the ladder is given by

$$I = \frac{V_{\text{ref}}}{2^{N_f} \cdot R_f + (2^{N_c} - 1) \cdot R_c} \tag{6}$$

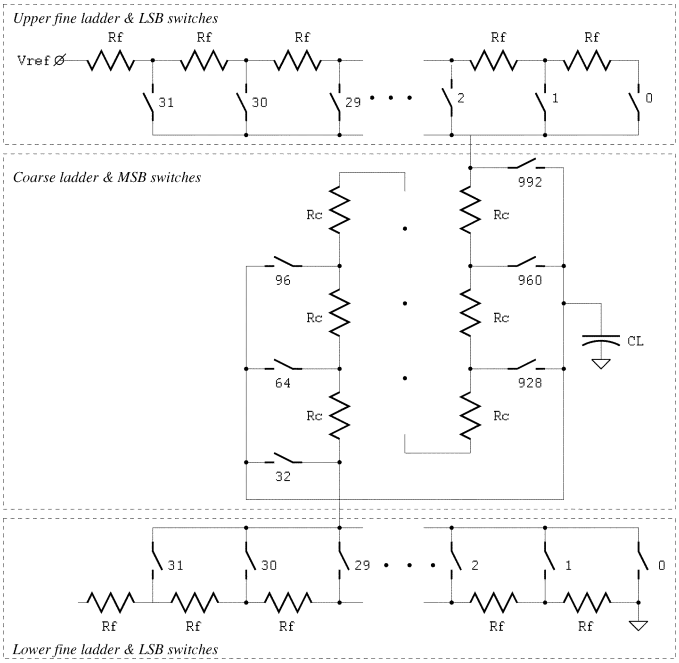


Fig. 3. "Inverted-ladder" DAC.

and the output voltage is

$$V_o = (L \cdot R_f + M \cdot R_c) \cdot I$$

where by L and M we denote the lower N_f and the higher N_c bits of the input code respectively. In order for the circuit to operate correctly, the following condition must be satisfied

$$2^{N_f} \cdot R_f = R_c. \tag{7}$$

Note that among similar equations, (1), (4), (7), the latter gives the smallest value for R_f compared to R_c, minimizing the penalty for the usage of the LSB ladder. In fact, when (7) holds, (6) can be written as

$$I = \frac{V_{\text{ref}}}{R_c + (2^{N_c} - 1) \cdot R_c} = \frac{V_{\text{ref}}}{2^{N_c} \cdot R_c}$$

and the output resistance (maximum at the middle code) can be written as

$$r_o = \frac{R_c \cdot 2^{N_c}}{4} = \frac{V_{\text{ref}}}{4 \cdot I}. \tag{8}$$

Indeed there is no increase in r_o due to the LSB ladder. The conclusion is that the inverted ladder is expected to give the best load-driving ability for a given power among the three presented.

Additional advantages of the proposed scheme are related to the switch matrix. First, we must note that the upper LSB ladder always operates close to V_{ref}, while the lower LSB ladder operates close to ground. Thus, higher LSB switches can be made of pMOS transistors only, while the lower switches made of nMOS. The immediate outcome is that the inter-ladder switch matrix in our scheme has half the parasitic switch capacitance compared to the current biasing scheme. Second, parasitic capacitors of the LSB switches have a very low driving resistance (i.e., Thevenin equivalent) as they are placed close to the supply rails. We are going to show that these switches can be made very large with negligible effect on the total equivalent parasitic capacitance.

Regarding the effect of switch resistance, there is always a single nMOS and a single pMOS switch in the string that carry static current. Thus, DNL is not affected by the switches, up to transistor matching and variations of the bulk biasing. The latter, however, is not significant, as the switches are placed close to upper/lower rails and exhibit only minor shift in bulk-to-source voltage. Large transistors are to be used in LSB switches, both to control the matching and to keep switch resistance low. To keep the DNL below half LSB, *absolute mismatch* of the switch resistance must be lower than $R_f/2$. Luckily, as we have mentioned earlier, LSB switches can be made very large with only a minor performance impact.

A drawback of the proposed scheme compared to the existing ones is that R_f has to be matched to R_c. In the passive scheme, they are completely unrelated, as long as the loading condition holds. In the current biasing scheme, the balancing condition can be satisfied by tuning I_f/I_c, even if there is a small deviation in $2^{N_f}R_f$. In our scheme, a mismatch between R_c and $2^{N_f}R_f$ results in DNL degradation at LSB ladder end points. Thus, R_f and R_c had better be made of identical unit resistances. That does not necessarily imply that there must be 2^N resistors, since R_f can be made of parallel-connected units, but the number of unit resistors can be large. DNL errors at LSB ladder end points can be also caused by systematic mismatch between the upper and the lower fine ladders. The two fine ladders must, therefore, be placed close to one another and drawn with appropriate layout techniques for mismatch control.

IV. Performance Comparison

We have evaluated the performance of the inverted ladder compared to current biasing and passive compensation schemes. Evaluation was carried out through numerical simulations (SPECTRE), with parasitics (except wire parasitics) included in the schematics. We have used a 3.3-V, 0.35-μm process with poly resistors.

The purpose of our evaluation was to determine the settling times of the testcases under given power consumption for various loads. For each of the three schemes, we have designed a 10-bit DAC, with N_f and N_c of 5. Every circuit was optimized once for 22-μA and once for 86-μA total current. Both the MSB and the LSB switch matrices were implemented in two levels: first level of eight 4-to-1 MUXes and second level of 8-to-1 MUX.[1]

MSB resistor area was adjusted to keep σ_{INL} of the middle tap below one LSB (about 0.7 LSB). In current biasing and passive compensation schemes the smallest possible LSB resistors were used. In the inverted ladder they were constructed from unit resistors matched to the MSB ladder: $R_f = R_u$, $R_c = 32R_u$.

[1]Dummy switches in passive-compensated DAC were accordingly sized to half of the MSB switches.

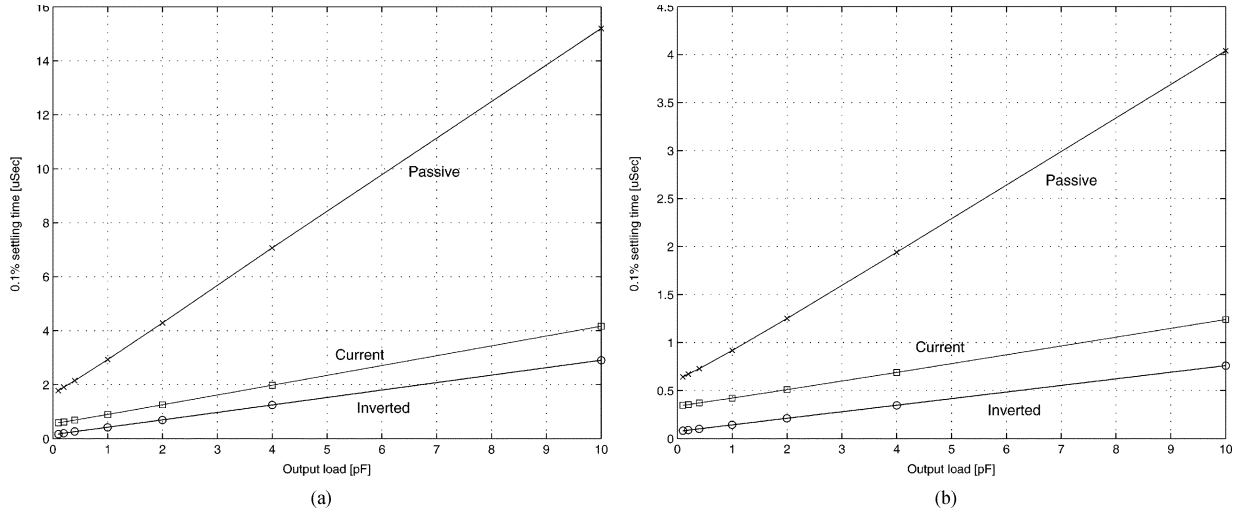


Fig. 4. 0.1% settling times versus output load. (a) 22-μA current. (b) 86-μA current.

The bias current I_f was determined according to the optimum calculated in (5); k was (optimistically) chosen to be 1. Equation (5) was verified by trying values slightly above and below the estimation and proved accurate.

Fig. 4 shows the 0.1% settling times versus output load for the tested circuits.

The settling time appears to have a linear dependence on the output load for a load capacitance above 100 fF. It can therefore be characterized by two parameters: the first is $r_{\rm eq}$, Thevenin equivalent resistance at the output node.[2] The other parameter is the equivalent parasitic capacitance C_p that must be added to the output load. The time constant is

$$\tau_0 = r_{\rm eq} \cdot (C_L + C_p)$$

and the settling time to half LSB precision is

$$t_s = 10 \ln(2) \cdot r_{\rm eq} \cdot (C_L + C_p). \tag{9}$$

Testcase circuit parameters are summarized in Table I, together with equivalent output resistance r_o and parasitic capacitance C_p.

The inverted ladder DAC shows a 25% imporvement in load driving ability for a given current, when compared to the current biasing scheme. Recalling the optimistic $k = 1$, which would be larger in a real implementation, we expect this gap to grow further. The inverted-ladder DAC also shows 3.5–4.5 times improvement in " parasitic delay," $\tau_0 = r_o C_p$, compared to current biasing. This is thanks to a much smaller C_p as it is effectively loaded only by MSB switch matrix, while the two others are loaded by both the MSB and the LSB matrices.

To prove the last point, we have tried loading the 22-μA DAC with large LSB switches: the switches were enlarged by a factor of 4 (i.e., brought to the sizes of the 86-μA DAC). The increase in C_p was barely noticed: it has risen to 545 fF from the 540 fF given in Table I.

[2]We have calculated Thevenin equivalents r_o for the three schemes, neglecting the switch resistance.

TABLE I
TESTCASE CIRCUIT PARAMETERS AND SIMULATED DYNAMIC PERFORMANCE

I_{total}	22μA			86μA		
DAC type	Passive	Current	Inverted	Passive	Current	Inverted
MSB res., [kΩ]	4.7	5.6	4.7	1.2	1.4	1.2
MSB res. L/W, [μm]	118/1.5	128/1.4	118/1.5	70/3.2	74/2.8	70/3.2
LSB res., [kΩ]	19	0.9	0.15	4.7	0.25	0.04
LSB res., L/W, [μm]	209/0.8	14/1	3.7/1.5	52/0.8	3.7/1	2.2/32
MSB switch, Wn, Wp [μm]	4, 6.4	3, 5	3, 5	16, 25.6	12, 20	12, 20
LSB switch, Wn, Wp [μm]	1, 1.6	3, 5	6, 10	6, 6.4	12, 20	24, 40
I_f [μA]		3.4			13.1	
r_o [kΩ]	196	52.2	38.9	49.6	13	9.9
C_p [pF]	1.2	1.5	0.54	1.7	3.7	1.07

V. FABRICATED PROTOTYPE

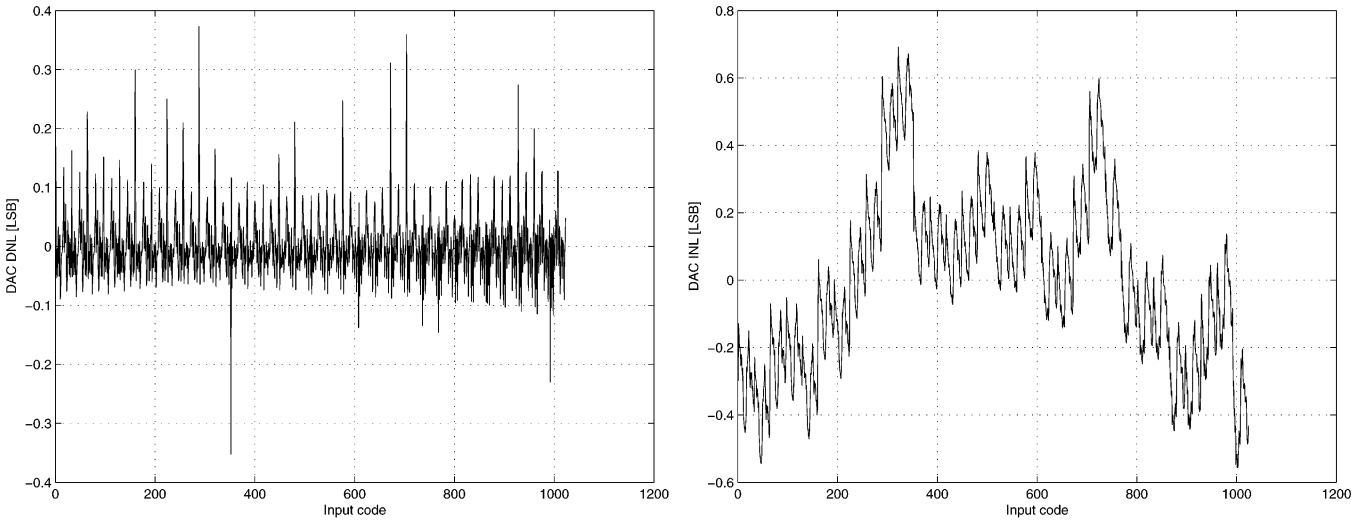
The proposed DAC was verified in silicon in a research chip for biological neural network interfacing. It was employed as a part of successive approximation A/D converters. It was loaded with 300-fF capacitive load.

The DAC designed for the test chip was very similar to the 22-μA testcase, with LSB switches twice smaller: for such a small output load the degradation in r_o was insignificant, but lower C_p resulted in somewhat better settling time.

After post-layout simulation the DAC showed r_o of 40.8 kΩ and C_p of 640 fF, some 100-fF increase due to wiring capacitance. Simulated output settling time constant for 300-fF load was about 38 ns. The layout area was 0.022 mm^2.

The chip was fabricated and proved fully functional. The actual time constant measured was 41 ns, which is indeed within the process parameters distribution. Fig. 5 shows the DNL and the infinite nonlinearity (INL) of a sample DAC. The layout is shown in Fig. 6. The peak INL measured was a bit higher than half LSB. It was caused by mismatch among MSB taps due to somewhat small area of MSB resistors, smaller, than required for 10-bit matching.[3]

[3]MSB resistors were deliberately made smaller than required for 10-bit matching, due to area requirements of the project. However, all the mentioned techniques must provide the same level of matching among the MSB taps, independent of how the secondary ladder is constructed. Thus, we feel that INL extending beyond half LSB does not derogate from the value of the contribution.



(a) (b)

Fig. 5. Test chip DAC nonlinearity. (a) DNL. (b) INL.

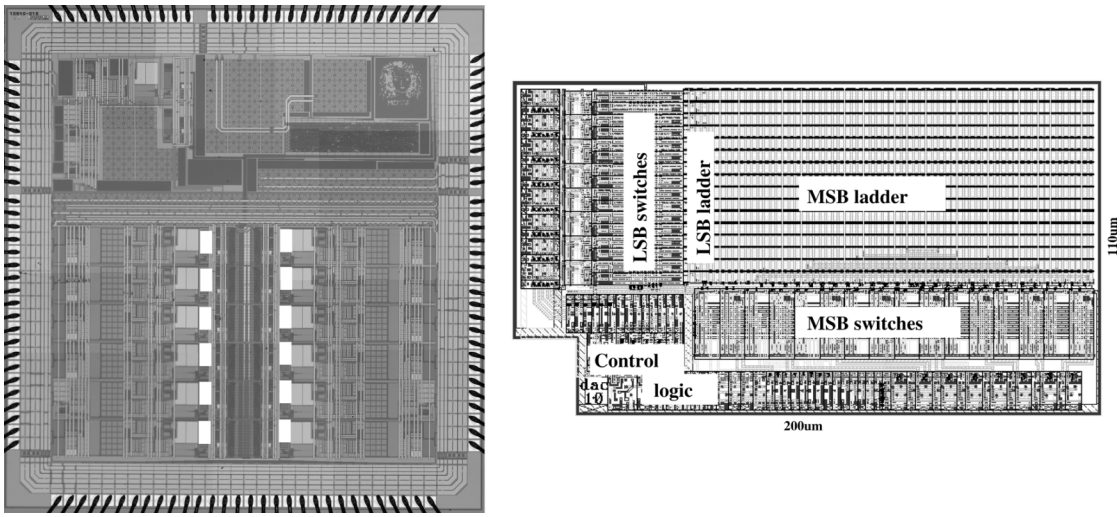


Fig. 6. Chip micgrograph (white squares placed over DACs) and DAC layout.

VI. Summary and Conclusions

We have presented a novel scheme of an inverted ladder DAC, where the MSB ladder floats upon the LSB ladder in opposite to existing circuits. It carries no active circuitry and is very simple to design. It was compared to existing schemes of current biasing and dummy-switch compensation through numerical simulations on a set of testcases. For a given current cosumption the inverted ladder digital-analog (D/A) provides significantly better load driving ability and up to four times lower parasitic delay.

A drawback of our scheme is that the LSB ladder is no longer independent of an MSB ladder. LSB ladder resistors must be matched with MSB ladder resistors to obtain good DNL. This may result in somewhat larger area consumed by the inverted ladder DAC and a more complicated layout, compared to the other schemes mentioned.

The inverted ladder D/A was fabricated on a 0.35-μm process and its performance was demonstrated to match the simulation resutls.

References

[1] B. Razavi, *Principles of Data Conversion System Design*. New York: IEEE Press, 1995.

[2] M. J. M. Pelgrom, "A 10-b 50-MHz CMOS D/A converter with 75-Ω buffer," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1347–1352, Dec. 1990.

[3] F. Maloberti, R. Rivoir, and G. Torelli, "Power consumption optimization of 8 bit, 2 MHz voltage scaling subranging CMOS 0.5-μm dac," in *Proc. IEEE Int. Conf. Electronics, Circuits, and Systems (ICECS '96)*, Rodos, Greece, Oct. 1996, pp. 1162–1165.

[4] L. E. Boylston, J. K. Brown, and R. Giger, "Enhacing performance in interpolating resistor string DACs," in *Proc. IEEE 45th Midwest Symp. Circuits and Systems, (MWSCAS '02)*, Aug. 2002, vol. 2, pp. 541–544.